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**AMENDMENTS TO THE CLAIMS**

1. (Currently amended) A fully depleted semiconductor-on-insulator (SOI) field effect transistor (FET), comprising:

    a layer of semiconductor material disposed over an insulating layer, the insulating layer disposed over a semiconductor substrate;

    a source and a drain formed from the layer of semiconductor material;

    a body formed from the layer of semiconductor material and disposed between the source and the drain, wherein:

        the layer of semiconductor material is etched such that a thickness of the body is less than a thickness of the source and the drain and such that a recess is formed in the layer of semiconductor material over the body, the body having a thickness of less than about 50 Å; and

        the source and the drain form junctions with the body such that no extensions are disposed between either of the source and body or the drain and the body; and

    a gate formed at least in part in the recess and the gate defining a channel in the body, the gate including a gate electrode spaced apart from the body by a gate dielectric made from a high-K material.

2. (Canceled)

*2* 3. (Original) The FET according to claim 1, wherein a spacer is formed adjacent each sidewall of the gate electrode.

*3* 4. (Original) The FET according to claim *3*, wherein each spacer is formed at least in part in the recess.

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*4* 5. (Original) The FET according to claim *3*, wherein each spacer is formed from an undoped polycrystalline silicon.

*5* 6. (Original) The FET according to claim *3*, wherein the spacers are respectively separated from the source and the drain by an oxide layer.

*6* 7. (Original) The FET according to claim *3*, wherein the spacers are separated from the gate electrode by the gate dielectric.

*7* 8. (Original) The FET according to claim 1, wherein the gate electrode is formed from a metal containing material.

*8* 9. (Original) The FET according to claim *8*, wherein the gate electrode is composed of one or more materials selected from aluminum, ruthenium, ruthenium oxide and mixtures thereof.

*9* 10. (Original) The FET according to claim 1, wherein a source contact is disposed over the source, a drain contact is disposed over the drain and a TEOS oxide layer is formed over the source contact and the drain contact.

*10* 11. (Original) The FET according to claim 1, wherein the high-K material of the gate dielectric has a relative permittivity of greater than about 20.

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~~12.~~ (Original) The FET according to claim 1, wherein the high-K material of the gate dielectric is composed of one or more materials selected from hafnium oxide; zirconium oxide, cerium oxide, aluminum oxide, titanium oxide, yttrium oxide, barium strontium titanate and mixtures thereof.

13-24. (Canceled)